EPA/EPO/OEB
D-80298 München
+49 89 2399-0
TX 523 656 epmu d
FAX +49 89 2399-4465

Europäisches Patentamt
European Patent Office
Office européen des brevets

Generaldirektion 2
Directorate General 2
Direction Générale 2

Eisenführ, Speiser & Partner
Martinistrasse 24
28195 Bremen
ALLEMAGNE

EISENFÜHR, SPEISER & PARTNER
EINGEGANGEN/RECEIVED
29. Mai 2002
+EBK
BREMEN
FRIST 10.09. ✓ ml Kxb
Frist: 12.08. N ml Kd-schrift?

Datum/Date 27.05.02

| Zeichen/Ref./Réf. | Anmeldung Nr./Application No./Demande n°./Patent Nr./Patent No./Brevet n°. |
|---|---|
| R 854 JOE/aw | 91908374.1-2201/0525068 |

Anmelder/Applicant/Demandeur/Patentinhaber/Proprietor/Titulaire
Rambus Inc.

**SUMMONS TO ATTEND ORAL PROCEEDINGS PURSUANT TO RULE 71(1) EPC**

You are hereby summoned to attend oral proceedings arranged in connection with the above-mentioned European patent.
The matters to be discussed are set out in the communication accompanying this summons (EPO Form 2906).

The oral proceedings, which will be public, will take place before the opposition division

and 11.09.02

* on 10.09.02 at 09h 00 hrs in Room 3468 at the EPO Bayerstr.34 *
* PschorrHöfe, D-80335 München *

No changes to the date of the oral proceedings can be made, except on serious grounds (see OJ 10/2000, p. 456).
If you do not appear as summoned, the oral proceedings may continue without you (Rule 71(2) EPC).
Your attention is drawn to Rule 2 EPC, regarding the language of the oral proceedings, and to the Official Journal 9/91, p. 489, concerning the filing of authorisations for company employees and lawyers acting as representatives before the EPO.
The final date for making written submissions and/or amendments (Rule 71a EPC) is ..12/08/02...... .

You are requested to report in good time beforehand to the porter in the EPO foyer. Room 3473 and 3474 are available as waiting rooms.
Parking is available free of charge in the underground car park.
However, this applies only in the case of accessing the car park via the entrance "Zollstrasse".

H. Schall

For the opposition division:
Tel. No.: (089) 2399-2647

Annexes:
Confirmation of receipt (Form 2936)
Rule 2 EPC (EPO Form 2043)
Communication (EPO Form 2906)

P6

Registered letter with advice of delivery

## ANNEX TO THE SUMMONS

### I. SUMMARY OF FACTS AND SUBMISSIONS

1). European patent No. 0 525 068 was granted on the European patent application No. 91 908 374.1 filed on 16.04.1991 and claiming priority from the US application serial No. 51 0898 filed on 18.04.1990. Publication and mention of the grant of the patent was made on 19.04.2000 in Bulletin 2000/16.

The Patent Proprietor is Rambus Inc.

2). Notices of oppositions were received from

Opponent O I: Micron Europe Ltd. and Micron Technology Italia S.R.L.
Opponent O II: Infineon Technologies AG
Opponent O III: Hyundai Electronics Deutschland GmbH, renamed into Hynix Semiconductor Deutschland GmbH
Opponent O IV: Micron Semiconductor Deutschland GmbH

in which revocation of the patent as a whole under Articles 100(a), (b), (c) were requested on the grounds that the subject-matter of the patent included added subject-matter, was not new, did not involve an inventive step, and that the European patent does not disclose the invention in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art. The opponents submitted an auxiliary request for Oral Proceedings.

In support of the requests to revoke the patent, the opponents cited a plurality of documents, and provided a sworn statement with respect to document **E1**.

These documents are indicated as E-documents in this ANNEX, the numbering of these documents as being indicated by the Patentee in his **"Anlage P6"**.

3). The Patent Proprietor requested the patent to be maintained without modification and all the oppositions to be rejected. The patent proprietor also submitted an auxiliary request for Oral Proceedings.

## II. NON-BINDING OPINION

**(With respect of claims 1 and 5)**

### A ADMISSIBILITY OF THE OPPOSITION FILED JOINTLY BY MICRON EUROPE LTD AND MICRON TECHNOLOGY ITALIA S.R.L. (OPPONENT O I)

1). According to Art. 99(1) EPC **any person** may give notice to the European Patent Office of opposition to the European patent granted.

The Patent Proprietor argued that the joint opposition filed by Micron Europe Ltd. and Micron Technology Italia S.R.L. **(O I)** is not admissible, because the wording "**any person**" should be interpreted as covering only a single legal person ("Rechtsperson"), so that each opponent has to pay the opposition fee according to Art. 99(1) EPC.

**Opponent O I** argued that two opposition fees were paid, so that the opposition is admissible.

2). According to the decision of the Enlarged Board of Appeal of 18 February 2002 (Case Number: **G 0003/99**), although the terms "joint opposition" or "common opposition" are not explicitly mentioned in the EPC, they correspond exactly to the situation dealt with in Rule 100(1), last sentence, EPC, which relates to "third parties acting in common in filing notice of opposition", "third parties" meaning simply a plurality of persons.

Further according to decision **G 0003/99**, the term "any person" in Article 99 EPC is to be construed in line with Article 58 EPC, so that as regards an opposition filed in common by a plurality of persons, each of the common opponents must be either a natural person, or a legal person, or a body equivalent to a legal person by virtue of the law governing it, or a combination thereof.

The Enlarged Board of Appeal argued that it follows from Rule 100(1) EPC (appointment of a common representative) that several persons acting in common in filing a notice of opposition are filing only one opposition and from Article 99(1),

last sentence, EPC, that only one opposition fee must be paid in due time in order for the opposition to be deemed to have been filed. The payment of the opposition fee is linked to the filing of one opposition and not to the number of persons who file the opposition. An opposition filed in common, apart from the fact that it is filed by more than one person, is as much a single opposition as an opposition filed by only one person. Consequently, the common opponents are obliged to act in common through their duly determined common representative.

3). **The Opposition division follows the argumentation of decision G 0003/99 and considers that the opposition commonly filed by Micron Europe Ltd. and Micron Technology Italia S.R.L. (O I) is admissible, independent of the fact that two fees have been paid.**

## B DISCLOSURE OF THE INVENTION (Art. 100 (b); Art. 83 EPC)

4). Claim 1 as granted relates to

a. a semiconductor memory device having at least one memory array which includes a plurality of memory cells, the memory device comprising:

b. clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54) having fixed frequency;

c. a programmable access-time register for storing a value which is representative of a number of clock cycles of the external clock signal (53, 54) to transpire after which the memory device responds to a read request;

d. a plurality of output drivers (76) for outputting data onto an external bus (18, 65) in response to a read request,

e. wherein the output drivers (76) output data on the external bus (18, 65) after the number of clock cycles of the external clock transpire and synchronously with respect to the external clock signal (53, 54).

5). With the semiconductor memory device according to claim 1, the **technical problem** is solved of how to modify a semiconductor memory device so that sufficient time is available to allow said device to perform an actual, desired memory read access, for example for a normal DRAM access this time must be longer than the row address strobe RAS time, so as to deliver the correct data (see **page 38, line 24 to page 39, line 12**).

To reduce the complexity of the slaves, a slave should preferably respond to a request in a specified time, sufficient to allow the slave to begin or possibly complete a device-internal phase including any internal actions that must precede the subsequent bus access phase.

The data block transfer occurs later at a time specified in an access time register, the time may be sent with the request packet control information, or already stored in the access time register. A device begins a data block transfer almost immediately with a device-internal phase as the device initiates certain functions, such as setting up memory addressing, before the bus access phase begins. The time after which a data block is driven onto the bus lines is selected from values stored in slave access-time registers.

6). Only Opponent **O I** contested that the subject-matter of claim 1 is insufficiently described contrary to **Art. 83 EPC**.

Opponent **O I** argued that, although the patent only discloses that a device always delays for a number of clock cycles dependent upon the value stored in the access time register, claim 1 appears to cover devices in which, if a specific value is stored in the programmable access time register, the device delays a predetermined number of clock cycles and outputs data synchronously with respect to the external clock signal, and in which, if another value is stored, the device does not delay.

7). This objection appears to relate to features c) and e).

The features a) to e) of granted claim 1 are disclosed in the original application in the following passages:

a. (pag 12, line 23 to page 13, line 6, and Figure 1);

b. page 57, lines 3 to 19, and Figure 12; page 46, line 19 to page 48, line 5, and Figure 8a, 8b;

c. page 14, lines 7 to 12: "semiconductor devices connected to the bus contain register ..... and access-time registers which store a set of one or more delay times at which the device can or should be available to send or receive data";

page 19, line 24 to page 20, line 9 (Protocol and Bus Operation), " the bus uses a relatively simple, split-transaction, block-oriented protocol for bus transactions; one of the goals of the system is to keep the intelligence concentrated in the masters, thus keeping the slaves as simple as possible", and "to reduce the complexity of the slaves, **a slave should preferably respond to a request in a specific time, sufficient to allow the slave to begin or possibly complete a device-internal phase including any internal actions that must precede the subsequent bus access phase, the time for this bus access phase is known to all devices on the bus, each master being responsible for making sure that the bus will be free when the bus access begins**";

page 21, lines 8 to 20, "the data block transfer occurs later at a time specified in the request packet control information, preferably beginning on an even cycle. A device begins a data block transfer almost immediately with a device-internal phase as the device initiates certain functions, such as setting up memory addressing, before the bus access phase begins. **The time after which a data block is driven onto the bus lines is selected from values stored in slave access-time registers**";

paragraph bridging pages 15 and 16, "a request packet and the corresponding bus access are separated by a selected number of bus cycles, allowing the bus to be used in the intervening bus cycles by the same or other masters for additional requests or brief bus accesses".

page 23, lines 4 to , "AccessType[1:2] (a field in the request packet 22, see Figure 4) preferably indicates the timing of the response, which is stored in an

access-time register, AccessRegN";

**page 39, lines 5 to 12,** "the value stored in a slave access-time register is preferably one-half the number of bus-cycles for which the slave device should wait before using the bus in response to a request".

**page 15,** "a master device, after seizing exclusive control of the external bus, initiates a bus transaction by sending a request packet to one or more slave devices on the bus. Each slave on the bus must decode the request packet to see if that slave needs to respond to the packet. The slave that the packet is directed to must then begin any internal processes needed to carry out the requested bus transaction at the requested time. A request packet and the corresponding bus access are separated by a selected number of bus cycles";

d. **page 53, line 24 to page 55, line 1, and Figure 10,** and

e. **page 58, lines 21 to 23, and Figure 13,** "the true and complement internal device clocks are also used to select which data is driven to the output drivers".

8) The cited passages with respect to features c) and e) thus define that a programmable access time register stores a value which is representative of a number of clock cycles of the external clock signal. The cited passages do not disclose that the device does not delay if another value is stored.

9). Because the aforementioned passages in the application have corresponding passages in the patent, it is the provisional, non-binding opinion of the opposition division that the European patent discloses the subject-matter of claim 1 in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art.

16). The subject-matter of the dependent claims appears to be disclosed in the passages as being indicated by the Patent Proprietor in his reply dated 22-05-2001, pages 16 to 18.

## C ADDED SUBJECT-MATTER (Art. 100(c); Art.123(2) EPC)

9). With respect of the ground of opposition relating to added subject-matter Art.123(2) EPC (**O I, II, III, IV**), the following has to be noted:

a). In the decision **T260/85** the Board of Appeal came to the conclusion that it is not permissible to delete from a claim a feature which the application as originally filed consistently presents as being an essential feature of the invention, since this would constitute a violation of Article 123(2) EPC. The application as originally filed contained no express or implied disclosure that a certain feature could be omitted, but that on the contrary the reasons for its presence were repeatedly emphasised in the application.

In the decision **T331/87**, the Board of Appeal held that the replacement or removal of a feature from a claim may not violate Article 123(2) EPC provided the skilled person would directly and unambiguously recognize that

(1) the feature was not explained as essential in the disclosure,

(2) it is not, as such, indispensable for the function of the invention in the light of the technical problem it serves to solve, and

(3) the replacement or removal requires no real modification of other features to compensate for the change: the feature in question may be inessential even if it was incidentally but consistently presented in combination with other features of the invention.

For this test for essentiality (or inessentiality) the relevant question is whether or not the amendment is consistent with the original disclosure.

This case law was confirmed in the decision **T136/88**.

10). All Opponents argued that the patent discloses subject-matter not disclosed in the application as originally filed on two counts, namely

a) **impermissible claim broadening**; and

b) **impermissible intermediate claim generalisations.**

11). With respect of a), **impermissible claim broadening**, the Opponents argued that the invention as originally disclosed was that as claimed in PCT claim 103, and that in the context of the overall description and it is the objective to provide devices, especially DRAMs, suitable for use with the bus architecture of the invention (see application, page 7:5-7). While granted claim 1 requires a semiconductor memory device including output drivers for "outputting data", PCT claim 103 explicitly required the device to interface to a **highly multiplexed bu** . The removal of this explicit requirement means that claim 1 does not require the data to be output onto a highly multiplexed bus, so that **claim 1 is broader than PCT claim 103.**

The Opponents further argued that in the **highly multiplexed bus system**, address, data and control signals are carried on the same bus lines, so that it is of course **important to ensure** that data resulting from the satisfaction of an earlier request **does not collide** on the bus with address and control information relating to a subsequent request. The Opponents also argued that in a **non-multiplexed bus system** where address data and control signals are carried on separate lines, data resulting from the satisfaction of an earlier request **cannot collide** with address and control information relating to a subsequent request. The modifiable access times are thus disclosed only as a consequence of the highly multiplexed bus and do not in the inventor's view have any existence independent of it.

12). It is the provisional, non-binding opinion of the Opposition Division that the subject-matter of granted claim 1 does not violate Article 123(2) EPC with respect of **impermissible claim broadening** for the following reasons:

a. The application as filed included a plurality of different inventions.

The invention remaining in the present application is mainly based on original **claim 103.** Claim 103 is directed to a semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices

connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines that the number of bits in a single address.

b. Using decision **T331/87**, the opposition division has the following opinion:

The question is whether the feature in **claim 103**, namely that the bus has substantially fewer bus lines than the number of bits in a single address, is a true limiting feature for the application of modifiable access-time registers in the memory device.

The application as filed discloses the "fewer bus lines" feature in the following context:

**page 11, line 25 to page 12, line 10** tells us that there is no need for separate device-select lines (in the bus) since device-select information for each device on the bus is carried over the bus, and that there is no need for separate address and data lines because address and data information can be sent over the same lines. These part of the description thus does not exclude the possibility that the bus does not have a reduced number of lines.

Furthermore, the application as filed does not mention any special necessary technical relationship between the reduced number of bus lines and the application of modifiable access-time registers. Although Figure 4 of the original description (see also pages 21 and 22) mentions a preferred embodiment, wherein a request packet 22 contains 6 bytes of data, 4.5 address bytes and 1.5 control bytes, and wherein each request packet uses all nine bits of the multiplexed data/address lines for all six bytes of the request packet, it is immediately clear to a reader of the original description that it is not essential for the concept of modifiable access-time registers in how many bytes the request packet should be transferred in a multiplexed way. It can be derived from Figure 4 that the ACCESSTYPE[0:3] field of the request is transferred in cycle 0-EVEN.

Furthermore, the application as filed does not disclose that the use of modifiable access-time registers is in technical consideration only possible with a bus having a reduced number of bus lines.

c. The application as filed mentions the data collisions in the following context:

According to **page 30 to 35 (Bus Arbitration)**, **"the (single) master can schedule multiple requests so that the corresponding data block transfers do not overlap", and**

**"in configurations with multiple masters, ..., where two or more masters send a request packet at about the same time and the multiple requests must be detected, they must sorted out by some sort of bus arbitration", and**

**"there are many ways for each master to keep track of when the bus is and will b busy".**

According to **page 22, lines 3 to 10**, "in a valid request packet, AddrValid 27 must be 0 in the last byte", and "asserting this signal in the last byte invalidates the request packet", and "this is used for collision detection and arbitration logic".

The chapter "Bus Arbitration" discloses several methods done by the masters to detect collisions, all methods being independent of the provision of the modifiable access registers in the slaves. According to **page 34, lines 4 to 9**, **"slave devices not need to detect a collision directly, but they must wait to do anything irrecoverable until the last byte (byte 5) is read to ensure that the packet is valid".**

13). With respect of point b), **impermissible intermediate claim generalisations**, the opponents (I) argue that the Technical Board of Appeal has settled case law on intermediate generalisation (**T284/94; T17/86**), namely that "an amendment of a claim by the introduction of a technical feature taken in isolation from the description of a specific embodiment is not allowable under Article 123(2) EPC if it is not clear beyond any doubt for a skilled reader from the application documents as filed that the subject-matter of the claim thus amended provides a complete solution to a technical probl m unambiguously recognisable from the application".

It was argued that granted claim 1 includes a technical feature that has been isolated from its original context and does not provide a complete solution to any technical problem disclosed in the originally filed application, because the introduction into granted claim 1 of the requirement for modifiable access times in respect of **read operations only** fails the condition as established by the Technical Board of Appeal, since according to the language of PCT claim 103, access time registers are set up prior to a request being made, this being consistent with the preferred embodiment of the invention, in which two access time registers are set up in advance (page 27: 1-15), and because the advantage of a modifiable access time register is to allow "**maximum utilisation of the bus for transfer of short blocks of data (application, page 16, not page 15:1-3)**, and because the device must have programmable access times in respect of all operations that require it to utilize the bus in response to a request.

14). It is the non-binding, provisional opinion of the Opposition Division that the objective technical problem solved by the subject-matter of claim 1 is how to modify a semiconductor memory device so that sufficient time is available to allow said device to perform an actual, desired memory access.

Indeed, from the description of the present application it can be understood that an advantage of using a modifiable access time register is the maximum utilization of the bus for transfer of blocks of data with respect of read and write requests, but this is not the object of the present invention.

Therefore, granted claim 1 must only require that the semiconductor memory device only needs to wait a predetermined period of time indicated by a value in an access register which is representative of a number of clock cycles of the external clock signal (53, 54) to transpire after which the memory device responds to a read request.

It is provisional, non-binding opinion of the opposition division that claim 1 does not suffer of impermissible intermediate generalisation.

15). With respect of claim 5, Opponents **O I and O III** object that the introduction of a delay locked loop in isolation amounts to **inadmissible intermediate**

generalisation contrary to Art. 123(2) EPC.

The Patent Proprietor argued that the claimed subject-matter (delay locked loop coupled to the clock receiver) is disclosed in the paragraph bridging original pages 56 and 57, and that this subject-matter is explained with respect of Figures 10, 12 and 13 on pages 57 to 59, line 2 (claims 78, 79, 108).

Opponent O I noted that the expression "delay locked loop" is not mentioned at all in the originally filed application.

The opposition division is of the provisional, non-binding opinion that claim 5 does not meet the requirements of Art. 123(2) EPC.

The following remarks have to be made:

a. Indeed the aforementioned expression has not been mentioned in the originally filed application.

b. Claim 5 depends on claim 3 or 4, thus it is defined that the clock receiver circuitry (101, 111) generates an internal clock signal (73) which clocks output drivers (76) after a predetermined number of clock cycles of the external clock transpire and synchronously with respect to a rising edge transition of the external clock signal.

c. It appears that it can not be concluded that, to achieve the synchronism with respect to the rising edge transition of the external clock signal, a "delay locked loop" is necessary.

d. Figure 12 is a block diagram showing how the internal device clock is generated from two bus clock signals using a set of adjustable delay lines.

It is not clear whether a "delay locked loop" is disclosed in the description of Figure 12.

17). The subject-matter of the other dependent claims is disclosed as being indicated by the Patent Proprietor in his reply dated 22-05-2001, pages 16 to 18.

## D Novelty (Art. 100(a); Art. 54 EPC)

18). According to the description of the application as filed, to reduce the complexity of the slaves, a slave should preferably respond to a request in a specified time, sufficient to allow the slave to begin or possibly complete a device-internal phase including any internal actions that must precede the subsequent bus access phase.

The data block transfer occurs later at a time specified in the request packet control information. A device begins a data block transfer almost immediately with a device-internal phase as the device initiates certain functions, such as setting up memory addressing, before the bus access phase begins. The time after which a data block is driven onto the bus lines is selected from values stored in slave access-time registers.

19). In this **ANNEX** the documents supplied by the Opponents have been indicated as E-documents, the numbering has been taken as being indicated by the Patent Proprietor as Anlage P6.

With respect of lack of novelty the following documents were mentioned:

**E1, E2, E3, E4, E5, E14, E17.**

It is noted that the opposition division considers these documents as the most relevant ones.

20). **E1 ("IC's for Entertainment ....")** mentioned by Opponents **O II and O III** appears to be not relevant with respect of novelty, independent of the fact that the sworn statement in writing is accepted that E1 has been published before the relevant priority date 18-04-1990.

**E1** discloses (see Figure 1 on page 9, and Figure 6 on page 14 and the description relating to these Figures) a two-chip Picture-in-Picture system consisting of **SDA 9088** - the **Picture Ins rtion Processor PIP** with the picture

memory as well as three D/A converters on chip, and the SDA 9087 - the Analog to Digital converter interface for the Inserted Picture (ADIIP). The **PIP** handles picture reduction, intermediate data storage in an integrated image memory (167,904 bits) , as well as the output of the decimated picture.

The SDA 9087 (Figure 2) adjusts an analog video channel to the digital input for the inserted picture of the picture processor SDA 9088.

Figure 3 shows the **SDA 9088 PIP,** comprising a PIP Memory (DRAM type) that is operated under I²C Bus control. According to pages 36 to 63 which relate to the PIP processor, the PIP processor combines two asynchronous picture sources so that a small moving picture (the inset picture) can be superimposed in a moving picture of normal size (the parent picture). The PIP memory has a capacity of bits large enough to store the data of the inset picture, and to output data that is synchronized with the parent channel. Data will be written in with the inset clock frequency and read out with the parent clock frequency (see Figure on page 40). The memory receives for reading out a clock signal from the **block "Parents Clocks", which on its turn receives the signals BLNP (Blanking Parents, for parent lines synchronisation), VSP (Vertical synchron parent, for parent field synchronisation), RC ( for RC network for PLL loop) and LLP3 (Line Locked clock parent).** Signals BLNP and RC are sent to Phase Locked Loop PLL, which is used for synchronizing the internally generated clock with the external line frequency of the parent channel.

The interface between the inset and parent channel is thus done by the on-chip PIP memory.

A SELECT output signal inserts the inset picture into the parent picture driving an external analog switch, eg. the TDA 4580.

The PIP memory DRAM contains two memory arrays which operate simultaneously to achieve high data rate of about 300 Mbits/s. **The total amount of data for one TV line is read out from both arrays in two memory cycles. First at the start of the insert position and second in the middle.** The operating speed of the memory is low, and there is an efficient parall l transfer of

large amount of data bits to and from the m mory c ll array via shift registers.

The $I^2C$ Bus interface works as a slave receiver and functions only if the inset clock LLI3 is available. The presence of an external clock is necessary for the operation of $I^2C$ Bus interface, namely signal SCL which is a serial clock. For the analog parent channel the LL3P clock is generated.

The $I^2C$ Bus interface comprises a register 2 to fine adjust the location of the inserted picture on the screen, and a register 3 used to control the read delay and the inset picture location as eg. upper right, upper left, lower left and lower right (see pages 46 to 48).

The four corners of the parent picture are foreseen as positions for inserting the inset picture. **To enable compatibility to different system configurations, readout from memory can be shifted horizontally in 63 steps by max. 252 LLP3 cycles and vertically in 15 steps by max. 30 lines in the parent field setting the control bits RDH and RDV in control register 2 and 3 (see also Table 6 on page 46).**

According to pages 47 and 48, in register 2 the bits d0-d3 indicate the read delay vertical in BLNP period, and in register 3 the bits d0-d5 indicate the read delay horizontal. BLNP appears to be the blanking signal for the parent picture, while BLNI is the blanking signal for the inset picture. BLNP and BLNI have to be considered as sync signals. BLNI is used for synchronisation for the inset source. In register 3, the values for d0-d5 are such that the horizontal read delays are done in 63 increments of 4 LL3P periods, so having a maximum of 252 LL3P cycles.

The PIP comprises block $I^2C$ Bus which only functions if the inset clock LL3I is available. This block is connected to bus lines SDA and SCL, and comprises the registers 0 to 4.

It is the opinion of the opposition division that in E1 the reading operation of the memory is not a response to a request, as in the present invention, but reading is done, delayed, with respect of the l ading slope of the horizontal parent line

synchronisation or HSP signal, so that in fact the read request for the PIP memory is delayed, and the memory is read out directly after the read request..

21). **E2 (Yamaguchi)** mentioned by all opponents describes a semiconductor memory device that provides a serial output in accordance with a clock signal from an external source, and that comprises a timing control circuit that controls the serial output operation, wherein the timing for starting the aforementioned output operation is set at will by specifying the number of cycles of the aforementioned clock signal required between activation by an activation control signal from an external source and the start of the serial output signal, and wherein a counter circuit obtains said number of cycles from an external source in synchronism with said activation control signal and then performs a count-down operation in accordance with the aforementioned clock signal.

In **E2** the activation control signal appears to be the external control signal RAS', which is the result of an access request, and the clock signal appears to be serial clock signal SC (see Figures 1 to 3).

a. **E2** discloses that a semiconductor memory device such as a dual port memory (used for image processing) is provided, as external control signals, row address strobe signal RAS', column address strobe signal CAS', write enable signal WE', data transfer control signal DT'/OE9, serial output control signal SOE', and serial clock signal SC.

b. **E2** further discloses that in a prior art semiconductor dual port memory device (see Figure 4 for the operation thereof), which is provided with a serial access port that is used for the serial input and output of memory data in units of word lines in a memory array, the read data transfer mode - where the read data is serially output - is recognized when the levels of the column address strobe signal CAS' and write enable signal WE' are high and the level of the data transfer control signal DT'/OE' is low when the level of the row address strobe signal RAS' changes from high to low.

Such a serial access port is provided with a serial input/output circuit SOI, which is connected to input/output t rminals SIO1 through SIO4.

c. E2 further discloses that at this time, the address AX of the word line to be read is provided to external terminals A0 to Ai in synchronism with the level of the row address strobe signal RAS' changes to low, and that the read signals from the memory cells that are connected to the selected word line are set up in the data lines. Also, in synchronism with the level of the column address strobe signal CAS' falling to low which occurs with a slight delay following the level of the row address strobe signal RAS' becoming low, the address AY of the first column that is to be output serially is supplied to external terminals A0 through Ai.

d. E2 also discloses that in the prior art semiconductor memory device, during the phase that RAS' and CAS' signals are low, the serial output operation begins when the level of the external control signal DT'/OE' returns to high. The timing for this returning to high of DT'/OE' is controlled by monitoring the output signal of a counter circuit while monitoring when the level of the serial clock signal SC becomes low, said counter circuit being provided in an external memory control circuit and counting the horizontal pixel location, said counter circuit being advanced by using the serial clock signal.

e. E2 further discloses that in the prior art semiconductor memory device, when the level of external control signal DT'/OE' is set back to high, a timing signal φdt is generated, and this timing signal is used to transfer to the data register of the serial access port the read data that had been in parallel output to each of the data lines - and along with that, an output operation is begun for the new serial data (data following (AX.AY) that has been transferred to the data register in accordance with the timing signal φc which is generated in synchronism with the serial clock signal SC.

f. E2 mentions the following problem existing in this prior art semiconductor memory device.

When the rate at which display data is serially output increases, it becomes difficult to maintain a synchronism between the rising of the level of DT'/OE' and signal SC: if the delay time involved in advancing the counter circuit using the serial clock signal SC, and the delay time involved in decoding and monitoring the output signal from the counter circuit begins to increase relative to the period of

the serial clock signal SC, then rising the level of the data transfer control signal DT'/OE' in synchronism with SC becomes difficult (see Figure 4: timing mismatch between DT'/OE' and SC, because the rising of DT'/OE' is delayed with respect of the rise in the level of SC).

This results in the **shortening of the duration of the timing signal φdt** which is used for transferring to the data register the read data from the cells that are connected to the newly selected word line, and thus results in an unstable serial data transfer operation.

g. **The solution for this problem includes that the clock signal position where the data transfer operation to the data register is to begin (generation of φdt) is to be specified at will in accordance with the counter value of a counter circuit in a memory control circuit TC (see Figure 1),** this in contrast to the operation of the prior art device (see Figure 4) wherein that timing signal φdt is generated when the level of data transfer control signal DT'/OE' is raised to high in synchronism with SC.

h. According to **E2**, when the dual port memory is in the data transfer mode, that is when the levels of the column address strobe signal CAS' and write enable signal WE' are high and the level of the data transfer control signal DT'/OE' is low and the level of the row address strobe signal RAS' changes from high to low, in synchronism with this change in level, the number of cycles of the serial clock signal SC required from activation until the start of the next data transfer on the serial read data is set in external terminals IO1 through IO4 used for data input and output.

i. The timing control circuit TC is provided with a counter circuit CTR which receives the data on the number of cycles via the data input/output terminals IO1 through IO4 and performs a count-down operation in accordance with the serial clock SC.

The counter circuit CTR receives a timing signal φcs which is generated in synchronism with the falling level of the row address strobe signal RAS', and receives a timing signal φcp. When the timing signal φcs is generated, the number of cycles ctrz is stored in the counter circuit CTR. Because then the output of

counter circuit CTR has an output other than "0", the timing signal φcp is generated for advancing the counter CTR.

When the counter value becomes "0", timing signal φdt is created.

(According to pages 23 and 24, in the random access mode, the dual port memory is activated when the level of the row address strobe signal changes from high to low. The X address signals AX0 through AXi which specify the word line are fed to the external terminals A0 through Ai, and the number of serial clock signal SC cycles ctrz which must elapse between the level of the row address strobe signal falling and the start of the serial output operation on the read data is fed to the external terminals IO1 through 4 used for data input and output. The number of cycles ctrz is determined by the counter value of said counter circuit which is included in a memory control circuit that is external to the dual port memory, and which is used for controlling the horizontal pixel location on a CTR. To explain, letting N1 represent the counter value corresponding to the last bit in one wordline worth of read data and N2 represent the counter value when the level of the row address strobe signal is to fall, the number of cycles ctrz is N1 - N2.)

Timing signal φdt is generated when the value of counter circuit CTR becomes "0", and the read that has been set in each of the data lines is transferred to data registers DR1 through DR4. Furthermore, timing signal φsr is generated in synchrony with the serial output control signal SOE' which controls the data output buffer DOB of the serial input/output circuit SIO.

The said data is then output by the serial input/output circuit SIO to the outside via serial input/output terminals SIO1 through SIO4 in accordance with timing signal φc (see page 27).

According to page 14, when the dual port memory is in the serial read operation mode, the external terminals IO1 through IO4 for data input and output are provided with the number of cycles the serial clock signal required for starting the serial output operation after the serial read operation mode is activated. The serial access port of the dual port memory comprises data registers DR1 through DR4

corresponding to the complementary data lines in each memory array, data selectors DSL1 through DSL4, pointer PNT, column address decoder SCD. The data registers include pieces of flip-flops for latching purposes. Switch MOSFETs for data transfer use are provided between the I/O nodes of said flip-flops and their corresponding noninverting signal line and inverting signal line of the complementary data lines. The timing signal φdt is supplied to gates of these MOSFETs.

Each bit of the data register is connected to a corresponding switch MOSFET of data selector DSL, for selectively connecting each bit of the data register with the common data line CDS used for serial input and output. Pointer PNT

j. Thus in **E2** the generation of timing signal φdt during the phase of driving out the data from the memory to a data register in the memory device, said phase of driving out preceding the time to drive the data onto the bus.

k. In **E2**, when the dual port memory is in the read data transfer mode, the data output buffer of the serial input/output circuit SIO is set in the operation mode when the level of the timing signal φsr from the timing control circuit TC becomes high.

l. The problem mentioned in **E2** that has to be solved is thus totally different.

m. According to the description of the original application, all information sent between master devices and slave devices is sent over the external bus. To allow the bus to be used in intervening bus cycles by the same or other masters for additional requests or brief bus accesses, a request packet and the corresponding bus access are separated by a selected number of bus cycles, Thus multiple, independent accesses are permitted, allowing maximum utilization of the bus for transfer of short blocks of data. Transfers of long blocks of data use the bus efficiently even without overlap because the overhead due to bus address, control and access times is small compared to the total time to request and transfer the block.

Th bus uses a relatively simple, synchronous, split-transaction, block-oriented

protocol for bus transactions.

To reduce the complexity of the slaves, a slave should preferably respond to a request in a specified time, sufficient to allow the slave to begin or possibly complete a device-internal phase including any internal actions that must precede the subsequent bus access phase.

The data block transfer occurs later at a time specified in the request packet control information. A device begins a data block transfer almost immediately with a device-internal phase as the device initiates certain functions, such as setting up memory addressing, before the bus access phase begins. The time after which a data block is driven onto the bus lines is selected from values stored in slave access-time registers.

n. The signal for driving a data block onto the bus lines is considered to be not comparable with the timing signal φdt, but more with the timing signal φsr (see Figures 2 to 4) which depends on serial output control signal SOE' and clock signal SC.

Furthermore, in E2 the purpose of the circuit depicted in Figure 1 is to provide a timing signal φdt that does not have a shortened duration.

22). E3/E3a (Hasegawa) mentioned by Opponent O III relates to a memory system that can access a plurality of storage device blocks with different operating times based on their respective optimal timing. If all of the storage device blocks were controlled with a single timing, all of the storage device blocks were operated according to the timing of the slowest storage device block.

In Figure 1 of E3a, the memory system uses two types of storage devices: device 6 is a high-speed device, and device 7 is a low-speed device, and receives a system address signal via address bus AB, . **Device 6 operates for an interval of three clocks φ, while device 7 operates for an interval of seven clocks φ. Access to the selected device is started always at φ1.** Access to one of said devices is detected by address decoder 1 receiving a system address signal from

bus AB. The detection signal m1, m2 is used as a selection signal for selector 5, so as to supply an initial value T1 or T2 to shift register 5 which loads the value according to timing signal $\phi 1$. **T1 and T2 are equivalent to the respective access times or operating times of the storage device blocks.** Output bits D7-D10 of the shift register are supplied to a timing detection circuit G1-G4. The timing detection circuit provides a strobe signal $\varphi 2$ for latch register 8, which receives read output signal Dout from device 6 or 7. The timing detection circuit further generates chip selection signals for the respective devices 6 and 7. Meanwhile the storage device side controlled by said timing control circuit is connected to data bus DEB via bidirectional buffer 9, which is connected to storage devices 6 and 7's data input Din and data output Dout, via the aforesaid latch register 8.

In operation, when a **system address signal** to select slow device is supplied to address decoder 1, output signal m2 is formed, so that initial value T2 is loaded in sync with load signal $\phi 1$ formed by m2 and clock $\phi$ in shift register 5. According t Figure 2, D7 and D8 become 1, and D9 and D10 become 0 per $\phi 1$. Value T2 is shifted to the right, thus D9 and D10 sequentially become 1, each delayed one clock by the shift operation. When the seventh clock $\phi$ arrives, D7 becomes 0. Outputs D7 and D8 are used to create $\phi 2$, which is used to clock latch register 8, which on its tum is coupled to a bus via buffer 9.

**In E3, access to the selected device is started always at $\phi 1$, T1 and T 2 are equivalent to the respective access times in the storage device blocks, and it is not explicitly disclosed whether the timing signal $\phi$ is an external clock signal or not, and a latch 8 (bistable circuit) is clocked and not output drivers are clocked by $\phi 2$, and it is not clear how the bidirectional buffer 9 is clocked. Because of end signal ACK, the system is an asynchronous system. E3 does not disclose that the memory system is a semiconductor device comprising the clock receiver circuitry, the programmable access-time register and the plurality of output drivers.**

**In the present invention the request packet and the corresponding bus access are separated by a selected number of bus cycles. To initiate a bus transfer ver th bus, a master sends out a requ st packet, which is a**

c ntiguous series of bytes containing address and control information. The data block transfer occurs at a time specified in the request packet control information.

E3 does not appear to destroy the novelty of claim 1.

23). **E4/E4a (Kumagai)** mentioned by Opponent **O III** discloses that in former computers the main storage unit MS maintained independent clocks, with respect to the clocks used by the storage control unit SCU that controls said MS or the instruction processor IP that receives data and instructions from said SCU and executes. In the control of the interface between SCU and MS, the SCU sends to the MS the activation signal and the signal that indicates the type of access. When processing by MS is completed, the MS carries out a completion report with respect to the SCU. For carrying out the time management of the processing of the MS, the SCU counts the passage of time, based on the type of access, and when a set time has elapsed, a signal is sent to MS that directs data sending. Furthermore, on the other hand, the processing speed, that is, the machine cycles, of the SCU and IP is made variable, or an MS with different operation specification is connected.

However, when separate clocks were provided in SCU and MS, there was the problem that control is difficult in high speed because SCU and MS are unsynchronized.

As a solution, the clocks of the SCU and the MS are made to be in common, in that the same clock as that of the SCU generates the control signal of the memory device within MS and the signal that sets the data. No circuit that synchronizes is necessary.

MS 4, when a request from the SCU 3 is received by MRQ 20, generates by means of MCR 51 a control signal 64 in response to the request, and said control signal 64 including RAS' 200 and CAS' 201 of Figure 2. MCR 51 (Figure 3) comprises latches 306-309 that store the number of cycles. With respect to Figure 4a and 4b, memory devices with the same operation specifications are connected to SCU with different machine cycles, wherein the machine cycles of Figure 4b

are regarded as double those of Figure 4a. The delay time TRCD of the CAS' from the RAS' is provides as the operation specification of the memory. In both cases the TRCDE must be made the same value, even if the machine cycles fluctuate. This is done by setting proper values in latches 306-309.

E4 does not appear to destroy the novelty of claim 1.

24). **E5 (Giga Bit Logic)** mentioned by Opponent **O III** discloses SRAM 12G014 (pages 2-3 to 2-12). The block diagram on page 2-3 shows a synchronous registered Random Access Memory comprising an input clock generator, an output clock generator, a memory array with row decoder, sense amplifiers and column decoder, and an output master/slave register clocked by the output clock generator. The output clock generator receives an external clock signal. The output clock generator also receives a signal on the MODE input. This signal (see page 2.5) determines the function of the output master/slave register. These functions are REGISTER MODE, LATCH MODE. In the LATCH MODE, the non-pipelined DATA OUT is fed through on the falling edge of the clock signal in the current cycle and latched on the next rising edge of the clock signal. This allows the data output to appear without waiting for the next rising edge of the clock signal.

E5 does not appear to destroy the novelty of claim 1.

26). **E14 (US-A-4 858 113; Sacardi)** mentioned by Opponents **O I** and **O IV** discloses in Figure 5 a block diagram of a memory device having variable tick delay VTD devices (Figure 6) connected with each port thereof. The VTD devices variably control the input and output operations of the memories to selectively delay these elements in order to align the data for processing in a selected sequence. Each VTD device includes a plurality of multiplexers the number of which is determined by the number of data bits. Each multiplexer has a plurality of serialled input registers and output registers connected therewith. The VDT has 64 bits of data input, 4 bits of data output, and 32 control bits c0-c31. The 64 bits of data are independently controlled as bytes by means of four control bits for each byte.

E14 does not appear to destroy the novelty of claim 1.

27). **E17 (The cydra 5 ...)** mentioned by Opponents **O II** and **O III** discloses that the only way to achieve high bandwidth with slow memory technology is to use multiple memory modules in an interleaved fashion. **E17** further discloses that in a normal, sequentially interleaved memory, with an interleave factor of M modules, every Mth word is in the same memory module (see also Figure 8a, showing the conventional assignment of memory locations to memory modules in a sequentially interleaved memory system with four modules, wherein a memory module is busy for four cycles when handling a request). **E17** also discloses that in the case of a sequential reference stream this ensures high bandwidth, since all modules are referenced before the same module is referenced again (see Figure 8b, with a sequential request stream for perfect operation)

**E17** further discloses that although interleaved memories can provide the bandwidth requirements of high-performance processors, they do not address the desire for short access times.

**E17** also discloses that in pseudo randomly interleaved memory architecture, instead of assigning every Mth word to the same memory module, the memory locations are assigned to the memory modules in a carefully engineered pseudo random fashion such that every reference sequence likely to occur in practice would be as uniformly distributed across the memory modules as would a truly random request sequence (see Figure 9a).

In a pseudo randomly interleaved memory architecture, a request arriving at a queue will experience a delay equal to the memory chip access time plus the tim spent waiting in line.

**E17** further discloses that what is of concern is the nondeterministic nature of the access time in the context of a processor architecture in which every operation is rigidly scheduled at compile time and in which the latency of every operation, including the memory operations, must be deterministic.

If the compiler consistently underestimates the access time, the processor will spend a significant fraction of its time in a frozen state. If the compiler consistently overestimates the access time, the schedules generated at compile time are

unnecessarily dilated.

The memory latency register MLR is a programmatically writable register that always holds the value of the memory latency assumed by the compiler when scheduling the currently executing code. The memory system uses the value in this register to decide whether the datum is early or late and, consequently, whether the datum should be buffered or the processor frozen. The MLR may for example set to the minimum possible memory access time of 17 numeric processor cycles, when executing scalar code with little parallelism and a low request rate. When the program is in an innermost loop, the MLR is set to the optimum value of 26 cycles to reflect the expected delay due to the higher request rate. The MLR allows the compiler to treat memory accesses as having a deterministic latency but to use different values for the latency in different portions of the code so as to always deliver near-optimal performance.

**E17** does not appear to destroy the novelty of claim 1.

## E INVENTIVE STEP (Art. 56; Art. 100(a) EPC)

28). With respect of the teachings of **E1 to E5, E14, and E17** the subject-matter of claim 1 appears thus to be novel.

According to Opponent **O I**, the subject-matter of claim 1 is not inventive with respect of the teachings of **E7 or E4**, and is not inventive with respect of the teachings of **E2 and E17.**

According to Opponent **O II**, the subject-matter of claim 1 is not inventive with respect of the teaching of **E17**.

According to Opponent **O III**, the subject-matter of claim 1 is not inventive with respect of the teachings of **E6 or E7**.

It is noted that the opposition division considers these documents as the most relevant ones.

It is the provisional, non-binding opinion of the opposition division that it is appears to be not obvious for a person skilled in the art to regard it as a normal option to derive the claimed subject-matter from the aforementioned documents **E2, E4, E6, E7, E17**, alone or in combination, in order to solve the problem posed, because each of these documents relates to the solution of a different problem.

**E2, E4 and E17** have already been discussed with respect of novelty

29). **E6 (Nakabayashi)** mentioned by Opponent **O III** discloses a delay element in the form of a variable word length shift register for outputting delayed input data. The input data is one-bit serial data, or may be a few-bit parallel. A bit length corresponding to a delay time of required data is preset in a bit length setting circuit 15. A control circuit 6 provides a write timing signal for the write address decoder of a memory device 3 and a read timing signal generating circuit 2. The read timing signal generating circuit 2 generates a read timing signal delayed from the write timing signal by a delay time corresponding to a bit length signal provided by the bit length setting circuit 15. The main object of the invention disclosed in **E6** is to provide a variable delay circuit in which the increase in power consumption can be reduced even if the required delay time is rendered to be too long.

The subject-matter of claim 1 appears to involve an inventive step with respect of the teaching of **E6**.

30). **E7 (Gamma)** mentioned by Opponents **O I and O III** discloses a memory controlling apparatus for controlling signal transfer between a memory and a processor for processing the data accessed to said memory. Means are available for retaining and storing time information based on the operating speed of at least said memory and said processor. Control means control the timing of signal transfer between said processor and said memory on the basis of said time information, and comprise first means responsive to said processor for transmitting a memory access signal EX to said memory and second means for transmitting in response to said memory access signal and to the time information to said memory a signal to command the memory to transmit data to said processor at a time subsequent to transmission of said memory access signal

which is determined by the operating speed of said memory and said processor.

E7 provides a solution for the problem that, in a prior art system having a timing system for the signal transfer in the interface between the processor and the main memory, the timing system is fixed for a given physical configuration, circuit configuration and control configuration.

The features of the solution resides in a controller 13 (see Figures 1 and 2), which sends out on a signal line 119 a signal **GFDR** for instructing the main memory to send the readout data to a databus 118, and sends out on a signal line 120 a signal **ADV** for instructing a read data register RDR in the processor to read the data sent through the data bus 118. The controller 13 comprises configuration registers 20 and 21 which retain identification flags m1, m2, m3 for the machine cycle of the processor and identification flags ta1, ta2, ta3 concerning the access time of the main memory cells. One of the "m" flags and one of the "ta" flags can be set through the signal line 117 during the initialization of the processor.

A control circuit 22 produces signals S0-S4 based on the identification flags.

The signal EX is applied to a reset terminal R of a counter 25. The counter thus starts to count a timing signal T2 which is in synchronism with the machine cycle, from the time point at which signal EX the level "0". The outputs of the counter are supplied to a decoder 26. The decoder 26 send timings Ci - Ci+6 (for example Ci is "1" when the counter counted five machine cycles) which are used in a control circuit 27 that produces signals GFDR, ADV, BSYR for combinations of the identification flags and said timing signals (for example when m1 and ta1 are set to "1", then GFDR is sent at timing Ci and ADV is sent at timing Ci+1).

The solution of E7 has the advantage that for a change of the main memory access time due to an increase of the main memory capacity or reconfiguration of the main memory, the time system of the main memory interface can be flexibly changed by changing the content of the configuration register in the processor.

The subject-matter of claim 1 appears to involve an inventive step with respect of the teaching of E7.

31). **E2 and E17** have been discussed with respect of novelty.

The subject-matter of claim 1 appears to involve an inventive step with respect of the combination of the teachings of these documents.

32). **E4** has been discussed with respect of novelty.

The subject-matter of claim 1 appears to involve an inventive step with respect of the teaching of **E4**.

4

Martinistrasse 24
D - 28196 Bremen
Tel. +49-(0)421-36 35 0
Fax +49-(0)421-337 8788 (G3)
Fax +49-(0)421-328 8631 (G4)
mail@eisenfuhr.com

Eisenführ, Speiser & Partner

ANLAGE P6

## Stand der Technik

Dokument D1 (Anlage D1): "IC's for Entertainment Electronics, Picture-in-Picture System", Siemens Aktiengesellschaft, München, Veröffentlichungsdatum: 1989;

Dokument D2 (Anlage D2): Japanische Patentpublikation (Kokai) 63-239676, veröffentlicht am 5. Oktober 1988 (Yamaguchi);

Dokument D2a (Anlage D2a): englische Übersetzung der Anlage D2;

Dokument D3 (Anlage D3): Japanische Patentpublikation (Kokai) 60-80193, veröffentlicht am 8. Mai 1985 (Hasegawa);

Dokument D3a (Anlage D3a): englische Übersetzung der Anlage D3;

Dokument D4 (Anlage D4): Japanische Patentpublikation (Kokai) 64-29951, veröffentlicht am 31. Januar 1989 (Kumagai);

Dokument D4a (Anlage D4a): englische Übersetzung der Anlage D4;

Dokument D5 (Anlage D5): "GaAs IC Data Book & Designers Guide", Firma Giga Bit Logic Inc., Newburry Park, USA;

Dokument D6 (Anlage D6): US 4,876,670 (Nakabayashi);

Dokument D7 (Anlage D7): US 4,499,536 (Gemma);
Dokument D8 (Anlage D8): DE 37 33 554 A1 (Western Digital);

Dokument D9 (Anlage D9): "A Synchronous Approach for Clocking VLSI Systems", IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 1, February 1982;
Dokument D10 (Anlage D10): US 4,763,249 (Bomba);

Dokument D11 (Anlage D11): US 4.360,870 (Mc Vey);

Dokument D12 (Anlage D12): "13-ns, 500-mW, 64-kbit ECL RAM using HI-BICMOS Technology", IEEE Journal of Solid-State Circuits, Vol. SC-21, N . 5, October 1986

Dokument D13: MC88200 - "Cache/Memory Management Unit User's Manual" veröffentlicht 1988, s. S.2 links unten)

Dokument D14: US 4,858,113 ("Saccardi"; veröffentlicht am 15. August 1989)

Dokument D15: US 4,637,018 ("Flora"; veröffentlicht am 13. Januar 1987)

Dokument D16: US 4,785,428 ("Bajwa"; veröffentlicht am 15. November 1988)

Dokument D17: Der Artikel "The Cydra 5 Deparmental Supercomputer, Design Philosophies, Decisions, and Trade-offs" (Ramakrishna), aus der Fachzeitschrift IEEE Computer, veröffentlicht 1989 (vgl. Copyright-Hinweis auf der Titelseite),

Dokument D18: US-Patent 4,813,005 (Redig) veröffentlicht am 14. März 1989,

Dokument D19: Der Artikel "Design of PLL-Based Clock Generation Circuits" (Jeong), aus IEEE J. of Solid-State Circuits, Vol. SC. 22, No. 2, April 1987 (vgl. Kopfzeile),

Dokument D20: Der Artikel "A 32-bit VLSI CPU with 15-MIPS Peak Performance" (Forsyth), aus IEEE J. of Solid-State Circuits, Vol. SC. 22, No. 5, Oktober 1987 (vgl. Kopfzeile),

Dokument D21: Der Artikel "A Variable Delay Line PLL for CPU-Coprocessor Synchronization" (Johnson), aus IEEE J. of Solid-State Circuits, Vol. SC. 23, No. 5, Oktober 1988 (vgl. Kopfzeile),

Dokument D22: Die Druckschriften aus dem Prüfungsverfahren des europäischen Abzweigungspatents 0 525 068, und zwar die US-Patentschriften 3,969,706; 4,205,373; 4,315,308; 4,449,207; 4,500,905; 4,654,655; 3,983,537; 4,247,817; 4,333,142; 4,470,114; 4,630,193; 4,764,846; 3,821,715; 4,646,270,

Dokument D23: Japanese Patent Application JP-A-01-236494, Published September 21, 1989, and English Translation ("Akimoto")

Dokument D24: Japanese Patent Application JP-A-01-284132, published November 15, 1989, and English Translation ("Kosugi").

Dokument D25: US Patent No. 4,481,572, Issued November 6, 1984 ("Ochsner")

Dokument D26: IEEE 1987 CUSTOM INTEGRATED CIRCUITS CONFERENCE, "Self Termination Low Voltage Swing CMOS Output Driver" ("Knight")

Dokument D27: US Patent No. 4,445,204, Issued April 24, 1984, ("Nishiguchi")

Dokument D28: German Patent Publication DE 37 42 487, Published July 1988, and English Translation ("Kawai")

EPA / EPO / OEB
D - 80298 München
089 / 2399 - 0
Tx 523 656 epmu d
Fax 089 / 2399 - 4465



## Wichtige Hinweise zur mündlichen Verhandlung

Das Europäische Patentamt verfügt über keine eigenen Dolmetscher. Diese müssen im Bedarfsfall von außerhalb, teilweise sogar aus anderen Ländern, beigezogen werden, was mit einem hohen Aufwand an Kosten und organisatorischen Vorbereitungen verbunden ist. Muß ein Verhandlungtermin kurzfristig abberaumt werden, können Kosten für bestellte Dolmetscher nicht mehr vermieden werden.

Es wird daher gebeten, eine Simultanübersetzung nur bei wirklichem Bedarf in Anspruch zu nehmen. Es wäre wünschenswert, wenn sich die Beteiligten (zweckmäßigerweise gleichzeitig mit der Terminabstimmung) auf die Benutzung einer Amtssprache einigen könnten. Bei Verständigungsschwierigkeiten sind die Mitglieder der Einspruchsabteilung bereit zu helfen.

Die von den Verfahrensbeteiligten bevorzugte (abgestimmte) Verhandlungssprache und ggf. eine notwendige Simultanübersetzung sind dem Amt möglichst vor der in Regel 2(1) EPÜ angegebenen Frist mitzuteilen.

(bitte umblättern)

## Important information concerning oral proceedings

The European Patent Office has no interpreters of its own. When interpreters are needed they have to be brought in from outside, sometimes even from other countries, which is costly and involves considerable organisation. If oral proceedings have to be cancelled at short notice, the cost of interpreters already engaged still has to be borne.

Please therefore make use of simultaneous interpreting facilities only where strictly necessary. If possible the parties should agree on an official language for the proceedings, preferably at the time when they arrange a date. The members of the Opposition Division will be willing to help should any communication problems arise.

The EPO should be told if possible before the period mentioned in Rule 2(1) EPC which language the parties prefer (agree on) and whether simultaneous interpreting facilities are required.

(please see overleaf)

## Très important Procédure orale

L'Office européen des brevets ne dispose pas de son propre service d'interprètes. Aussi fait-il appel le cas échéant à des interprètes de l'extérieur, qui viennent même parfois de l'étranger, ce qui occasionne des frais élevés et demande un grand travail d'organisation. Si la date d'une procédure orale doit être annulée au dernier moment, il n'est plus possible d'éviter les frais d'interprètes.

Les parties à une procédure sont donc priées de ne demander une traduction simultanée qu'en cas de réel besoin. Il serait souhaitable qu'elles puissent se mettre d'accord en même temps qu'elles conviennent de la date sur l'utilisation d'une langue officielle comme langue des débats. Si les parties éprouvent des difficultés de compréhension lors des débats, les membres de la division d'opposition sont disposés à leur prêter leur assistance.

L'Office doit être avisé si possible avant le début du délai mentionné dans la règle 2(1) CBE de la langue préférée par les parties pour le déroulement des débats (et sur laquelle elles se sont préalablement mises d'accord) et de la nécessité éventuelle d'une traduction simultanée.

(voir au verso)